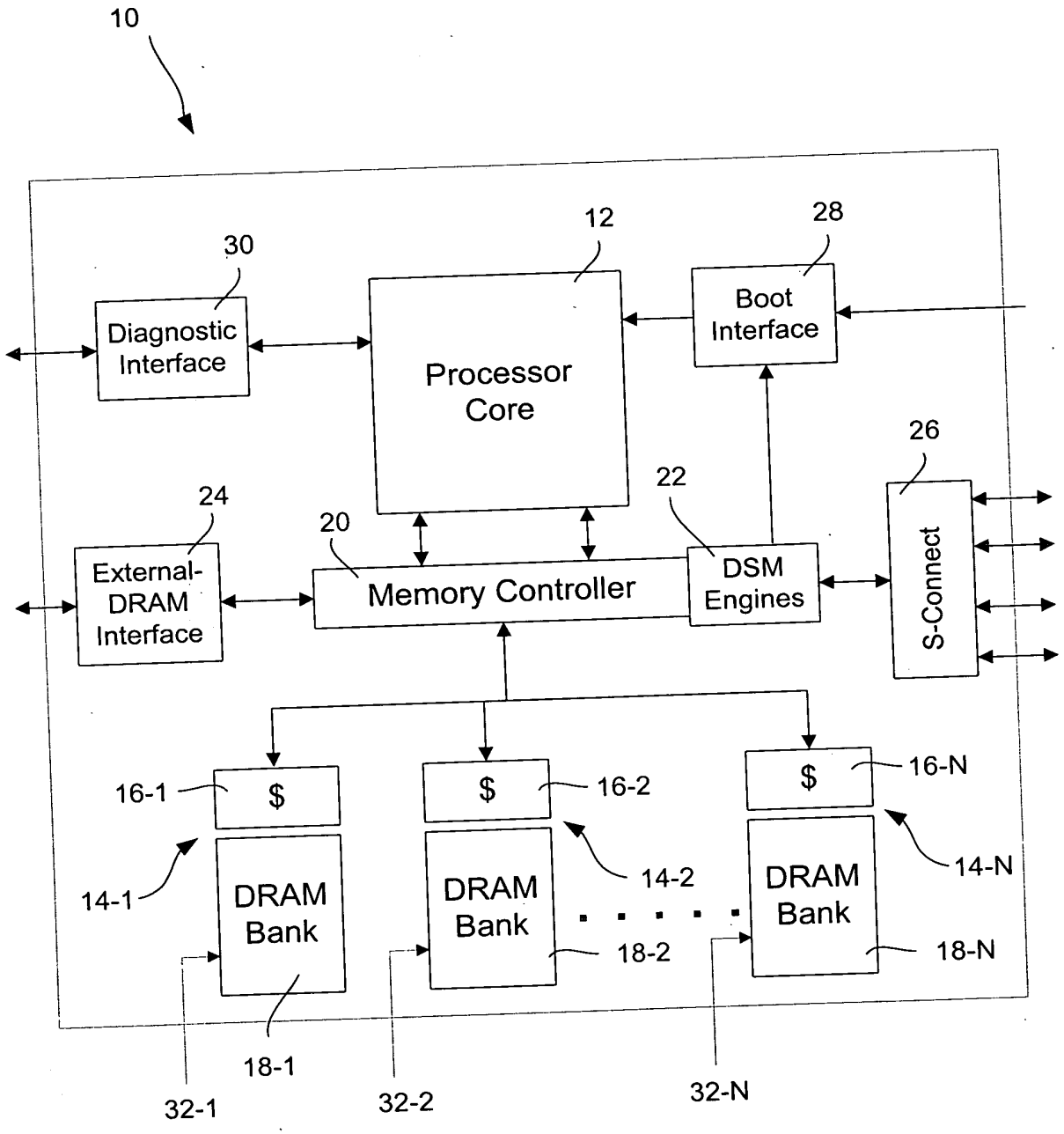
10
12
28
30
Diagnostic Interface
Processor Core
Boot Interface
26
24
22
20
External-DRAM Interface
Memory Controller
DSM Engines
S-Connect
16-1
$
16-2
$
16-N
$
14-1
DRAM Bank
14-2
DRAM Bank
14-N
DRAM Bank
18-2
18-N
18-1
32-1
32-2
32-N

Fig. 1

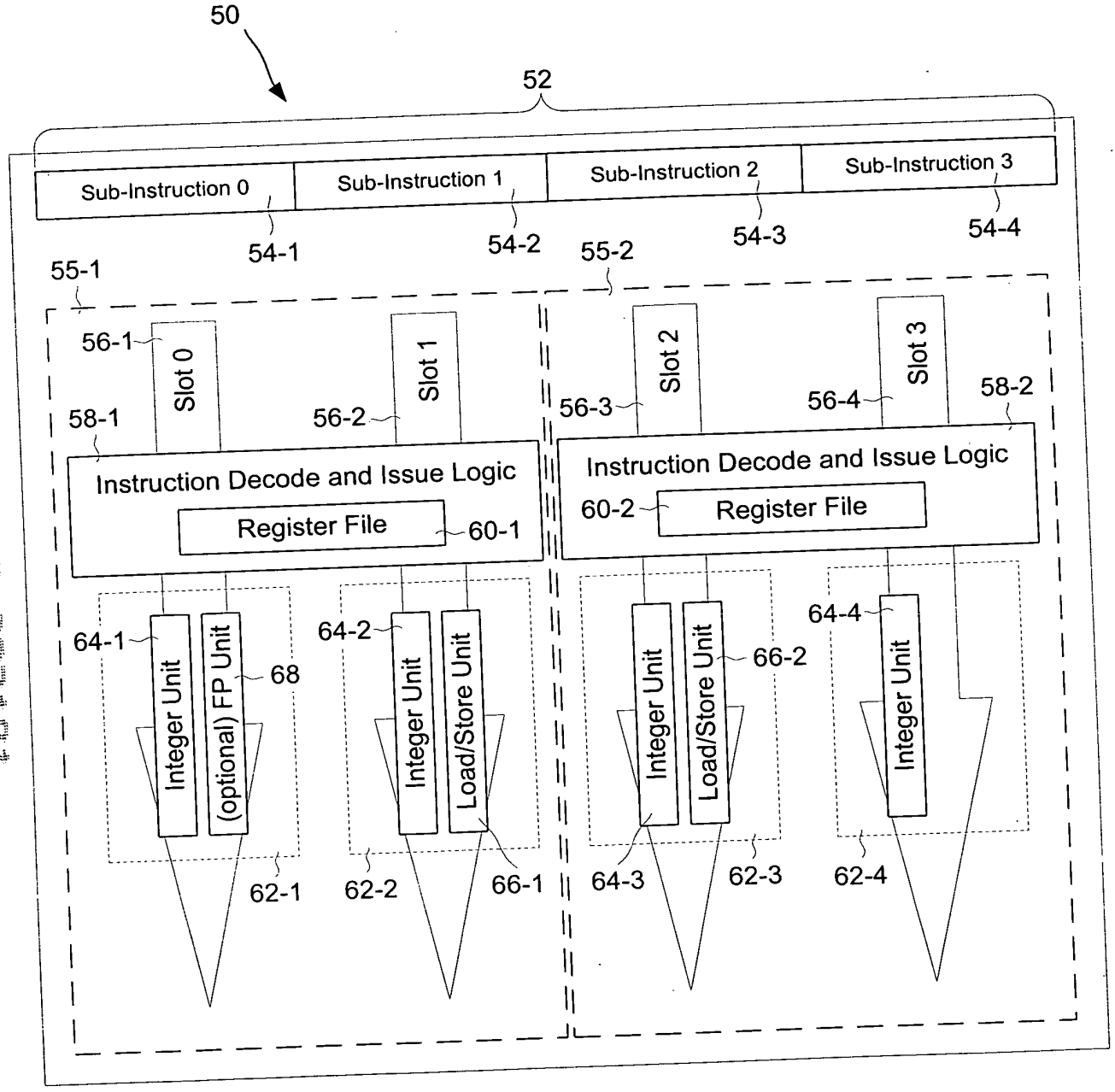
50
52
Sub-Instruction 0
Sub-Instruction 1
Sub-Instruction 2
Sub-Instruction 3
54-1
54-2
54-3
54-4
55-1
55-2
56-1
Slot 0
56-2
Slot 1
56-3
Slot 2
56-4
Slot 3
58-1
58-2
Instruction Decode and Issue Logic
Register File
60-1
60-2
64-1
Integer Unit
(optional) FP Unit
68
64-2
Integer Unit
Load/Store Unit
66-1
64-3
Integer Unit
Load/Store Unit
66-2
64-4
Integer Unit
62-1
62-2
62-3
62-4

Fig. 2

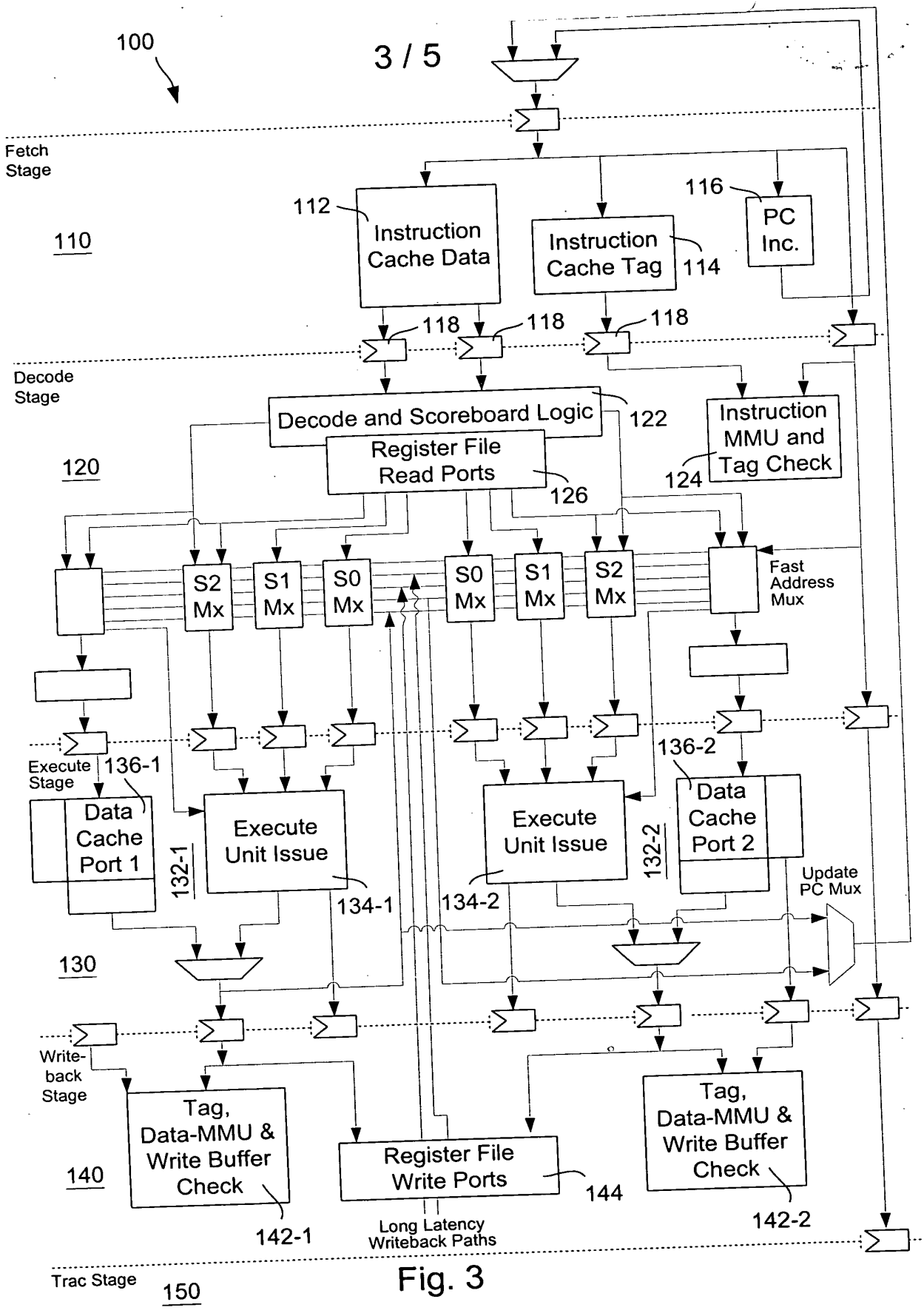
100
Fetch Stage
110
112
Instruction Cache Data
Instruction Cache Tag
114
116
PC Inc.
118
118
118
Decode Stage
120
Decode and Scoreboard Logic
122
Register File Read Ports
126
Instruction MMU and Tag Check
124
S2 Mx
S1 Mx
S0 Mx
S0 Mx
S1 Mx
S2 Mx
Fast Address Mux
Execute Stage
136-1
136-2
Data Cache Port 1
132-1
Execute Unit Issue
134-1
Execute Unit Issue
134-2
132-2
Data Cache Port 2
Update PC Mux
130
Write-back Stage
Tag, Data-MMU & Write Buffer Check
140
142-1
Register File Write Ports
144
Long Latency Writeback Paths
Tag, Data-MMU & Write Buffer Check
142-2
Trac Stage
150

Fig. 3

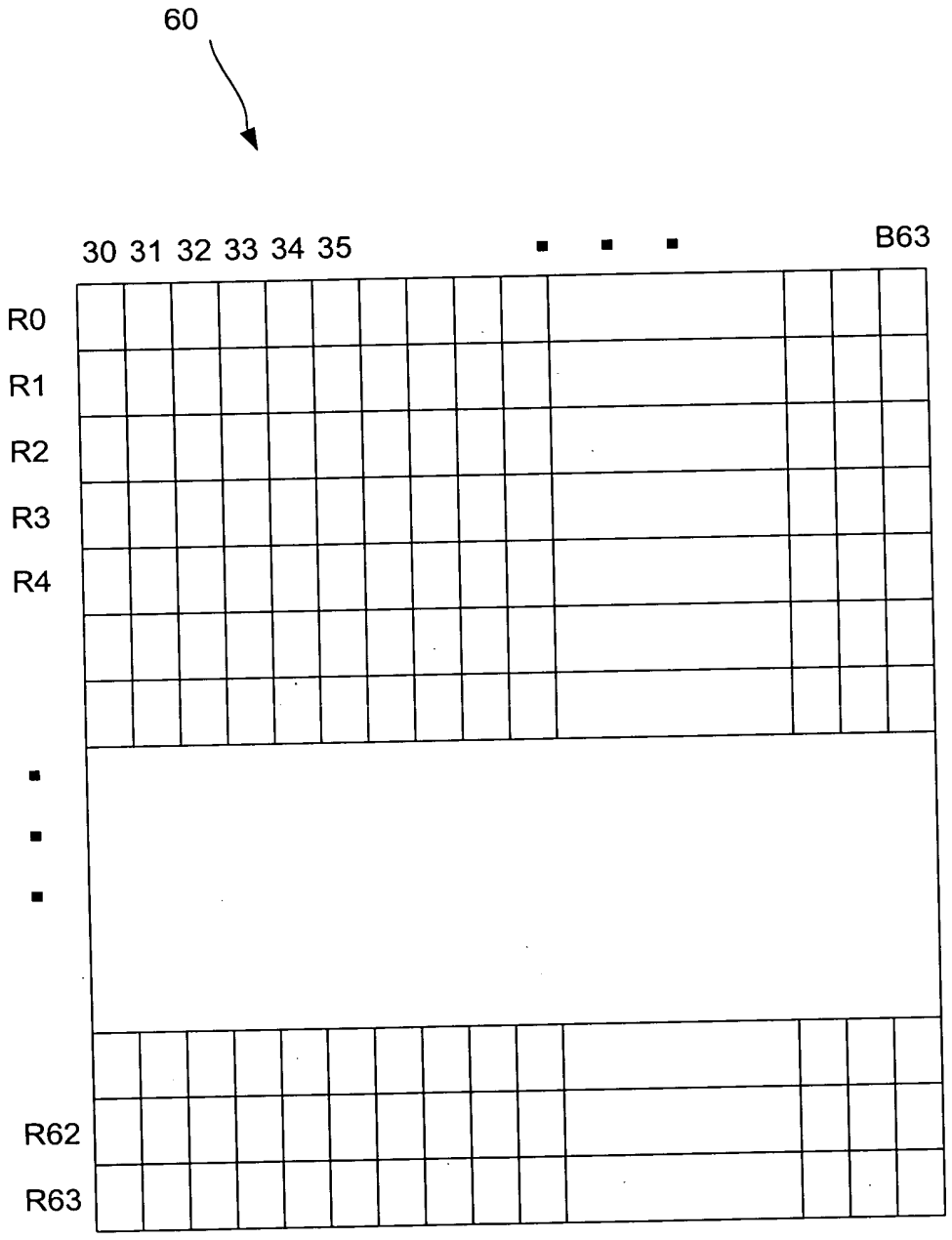

Fig. 4

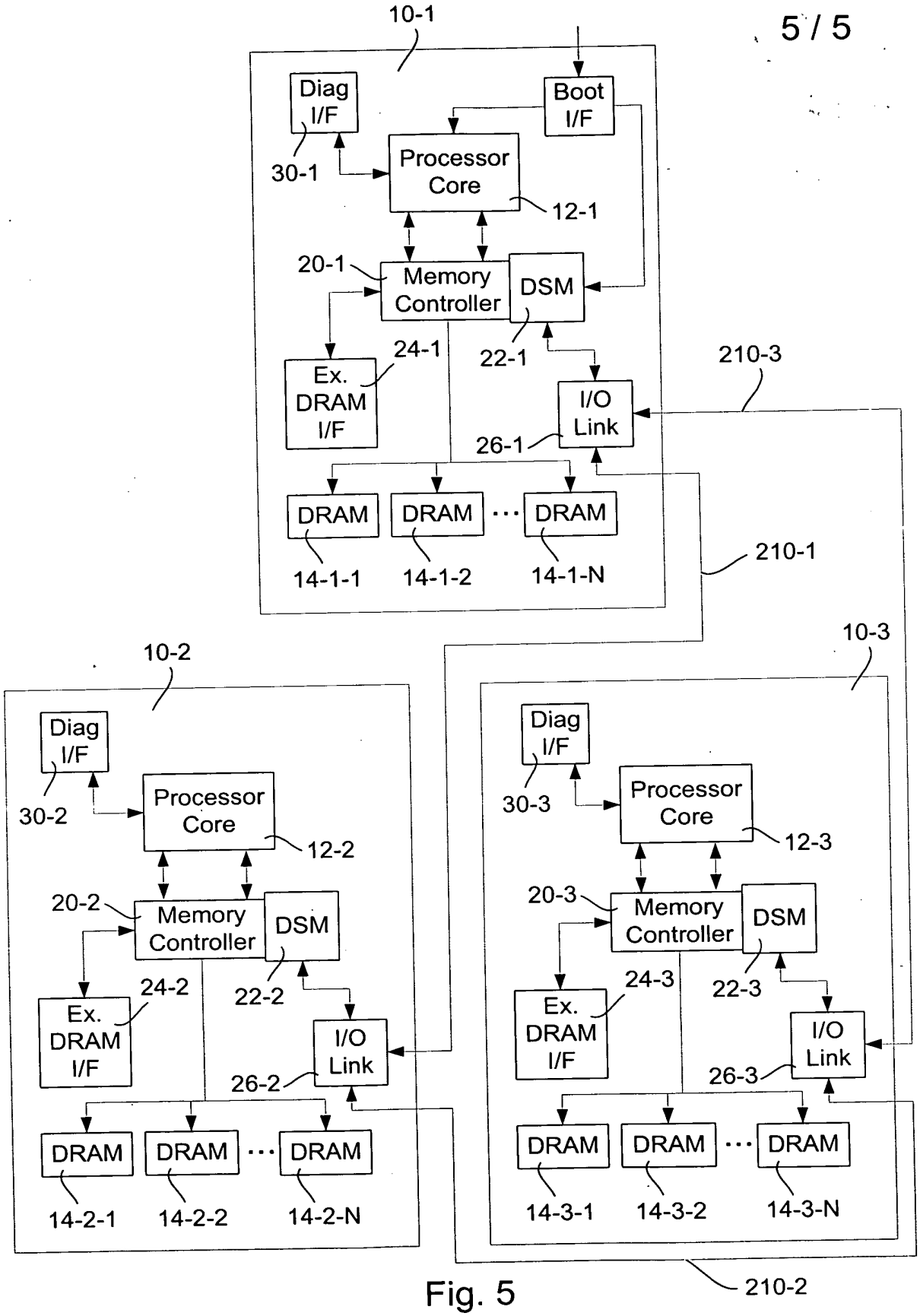
10-1
Diag I/F
30-1
Boot I/F
Processor Core
12-1
20-1
Memory Controller
DSM
22-1
24-1
Ex. DRAM I/F
210-3
I/O Link
26-1
DRAM
DRAM
DRAM
14-1-1
14-1-2
14-1-N
210-1
10-2
Diag I/F
30-2
Processor Core
12-2
20-2
Memory Controller
DSM
22-2
24-2
Ex. DRAM I/F
I/O Link
26-2
DRAM
DRAM
DRAM
14-2-1
14-2-2
14-2-N
10-3
Diag I/F
30-3
Processor Core
12-3
20-3
Memory Controller
DSM
22-3
24-3
Ex. DRAM I/F
I/O Link
26-3
DRAM
DRAM
DRAM
14-3-1
14-3-2
14-3-N
210-2

Fig. 5